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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,805	03/04/2004	Katsuhiko Shishido	69804-013	5235

7590 03/13/2006

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EXAMINER	
MATISIAK, JENNIFER E	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,805	SHISHIDO ET AL.	
	Examiner	Art Unit	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 21 is/are allowed.

6)☒ Claim(s) 1-3,8,9 and 20 is/are rejected.

7)☒ Claim(s) 4-7 and 10-19 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02232006.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

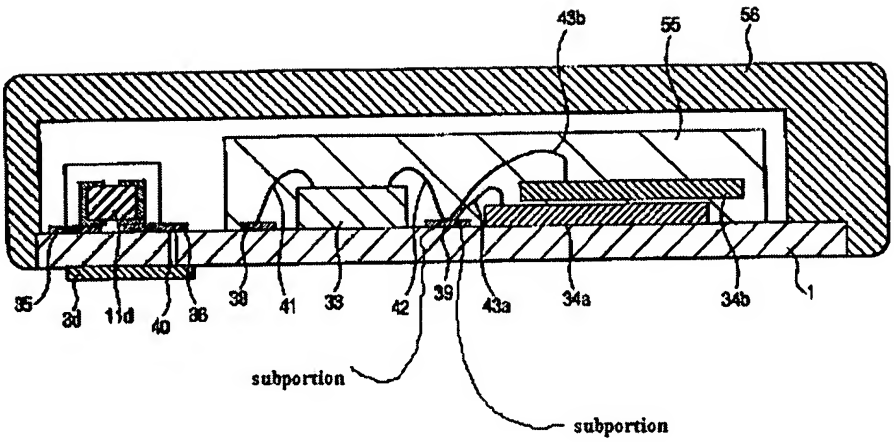
1. Claims 1-3, 8-9 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al. (US 2001/0011766), hereinafter Nishizawa.

Regarding claim 1, Nishizawa discloses a semiconductor device (Fig. 6, for example) including a plurality of layers of semiconductor chips (34a, 34b) having substantially the same outer contour with an integrated circuit being formed on a principal face of each semiconductor chip, comprising: a non-conductive layer having (1) a conductive portion provided thereon (39), and an internal connection member (43b) for internally connecting the integrated circuits formed on the plurality of semiconductor chips via the conductive portion provided on the non-conductive layer, wherein the conductive portion provided on the non-conductive layer only mediates internal connection between the integrated circuits formed on the plurality of semiconductor chips.

Regarding claim 2, Nishizawa discloses a semiconductor device wherein, the plurality of semiconductor chips comprise a first semiconductor chip (34b) and a second semiconductor chip (34a), and the internal connection member comprises: a first connection member (43b) for connecting the first semiconductor chip to the conductive portion; and a second connection member (43a) for connecting the second semiconductor chip to the conductive portion.

Regarding claim 3, Nishizawa discloses semiconductor device wherein the non-conductive layer has a circuit formed thereon (33), and the conductive portion comprises a conductive sub-portion (39, see figure below) which is connected to the first connection member (43b) and a conductive sub-portion (39, see figure below) which is connected to the second connection member (43a), the conductive sub-portions being in electrical conduction by way of the circuit formed on the non-conductive layer.

FIG. 6



Regarding claim 8, Nishizawa discloses a semiconductor device wherein the non-conductive layer (1) is a mount on which the plurality of semiconductor chips are placed.

Regarding claim 9, Nishizawa discloses a semiconductor device wherein the conductive portion (39) is formed with a conductive material (para [0113]), a portion of the non-conductive layer (1) that lies outside of an outer contour of the plurality of semiconductor chips when the plurality of semiconductor chips (34a, 34b) and the non-conductive layer are layered in place.

Nishizawa does not explicitly disclose "wherein the conductive portion is formed by plating." However:

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

Therefore, no patentable weight is given to the product-by-process claim limitation because the device disclosed in the invention of Nishizawa and the device of the instant invention are structurally equivalent.

Regarding claim 20, Nishizawa discloses a semiconductor device wherein, the second semiconductor chip (34a) is disposed so that a principal face of the second semiconductor chip not bearing the integrated circuit contacts a principal face of the non-conductive layer, the semiconductor device further comprising: a spacer (55) having an outer contour which is smaller than an outer contour of the first semiconductor chip and the second semiconductor chip, the spacer being disposed on the principal face of the second semiconductor chip having the integrated circuit formed thereon, and the first semiconductor chip (34b) is disposed so that a principal face of

the first semiconductor chip not bearing the integrated circuit contacts an upper face of the spacer (55).

Allowable Subject Matter

2. Claims 4-7, 9-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claim 21 is allowed. No prior art on record or combination thereof teaches the limitation "a non-conductive layer having a first conductive portion and a second conductive portion provided thereon wherein the second conductive portion provided on the non-conductive layer is a terminal for connecting the integrated circuits formed on the plurality of semiconductor chips to an external circuit."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DOUGLAS W. OWENS
PRIMARY EXAMINER

JEM